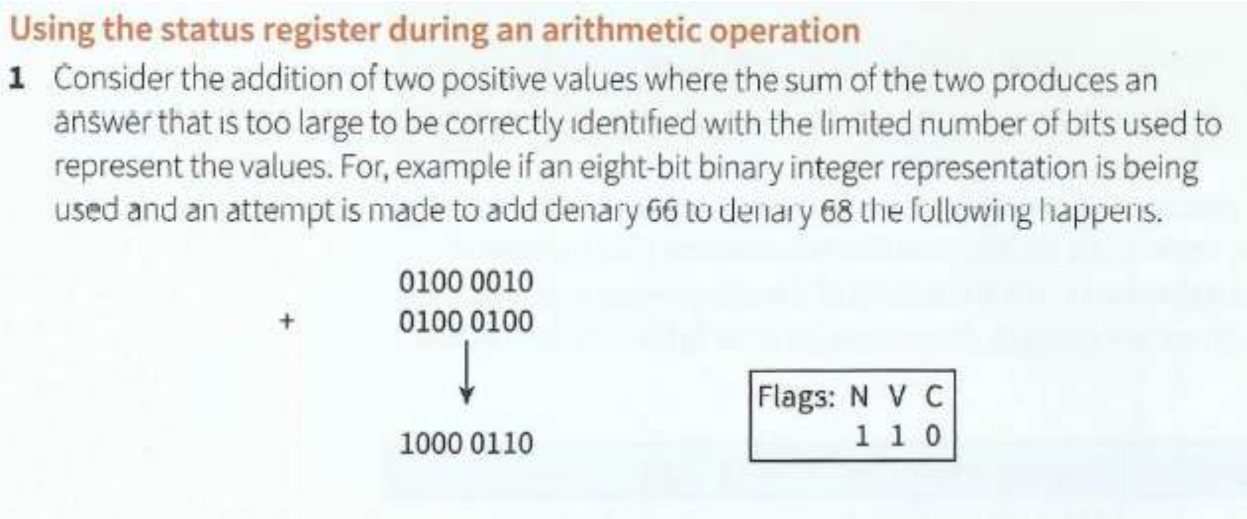
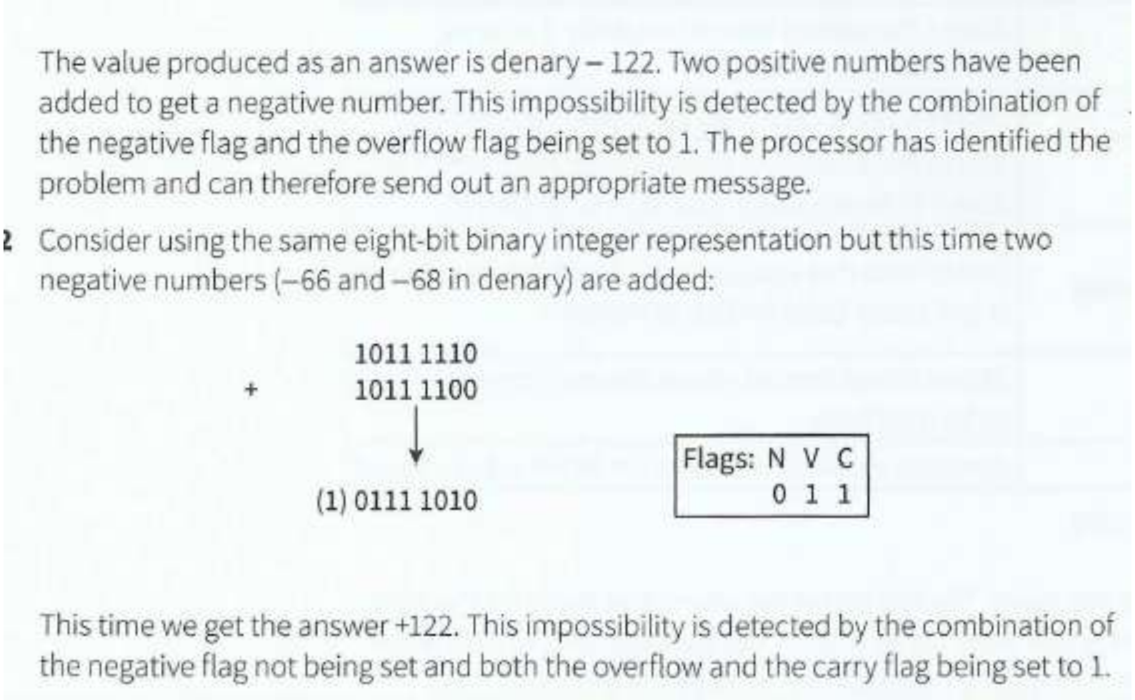


Using the status register during an arithmetic operation

1 Consider the addition of two positive values where the sum of the two produces an answer that is too large to be correctly identified with the limited number of bits used to represent the values. For, example if an eight-bit binary integer representation is being used and an attempt is made to add denary 66 to denary 68 the following happens.

```
      0100 0010
+     0100 0100
          ↓
      1000 0110
```

Flags:	N	V	C
	1	1	0



The value produced as an answer is denary – 122. Two positive numbers have been added to get a negative number. This impossibility is detected by the combination of the negative flag and the overflow flag being set to 1. The processor has identified the problem and can therefore send out an appropriate message.

2 Consider using the same eight-bit binary integer representation but this time two negative numbers (–66 and –68 in denary) are added:

```
          1011 1110
+         1011 1100
              ↓
      (1) 0111 1010
```

Flags:	N	V	C
	0	1	1

This time we get the answer +122. This impossibility is detected by the combination of the negative flag not being set and both the overflow and the carry flag being set to 1.